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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,822	10/29/2003	Taro Fujii	8017-1105	6783

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EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,822	FUJII ET AL.	
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/03, 5/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, declaration, and information disclosure statement, all filed 29 October 2003; and a second information disclosure statement filed 24 May 2004.

Priority

3. Applicant's claim for foreign priority date 30 October 2002 is hereby acknowledged.

Title

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims below are objected to because of the following informalities:

In general, claim language should be revised to improve readability, comprehensibility and grammar. Doing so may increase enforceability of any future patent that results from this application.

Claims 7 and 8, line 2: all of line 2 (in each claim) is unnecessary. This limitation has already been included in claim 6, upon which both claims 7 and 8 depend.

Claims 15, 16 and 17, line 3: the phrase "correspond in number" is unclear, as any two numbers can have a correspondence. For purposes of examination, the phrase will be interpreted to mean that there exists a state control unit for each element area. Applicant is advised to refine claim language to remove uncertainty.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Katsuki et al. (U.S. Patent No. 5,581,767) hereinafter referred to as Katsuki.

10. As per claim 1, Katsuki discloses an array-type processor in which

a multiplicity of processor elements (Fig. 1 processors 12), which individually execute data processing and supply event data as output in accordance with instruction codes for which data are individually set, *The examiner asserts that the processors process data and any results produced constitute event data.*

are arranged in rows and columns; *Fig. 1 shows processors 12 in rows and columns.*

and in which said instruction codes of this multiplicity of processor elements are successively switched by a state control unit (Fig. 1 controller block 22) in accordance with a computer program that has been installed in advance and said event data; (Col. 7 lines 38-46) wherein:

said state control unit is composed of a plurality of units that intercommunicate to realize linked operation as necessary; *Fig. 1 discloses multiple controller blocks interlinked to communicate.*

and said array-type processor includes an event distributing means (Fig. 1 bus 24) for distributing said event data to said plurality of state control units that intercommunicate and realize linked operation. (Col. 7 line 47 – col. 8 line 4)

11. As per claim 2, Katsuki discloses an array-type processor according to claim 1, wherein said event distributing means is constituted by dedicated event communication lines that connect said plurality of state control units. (Col. 7 line 47 – col. 8 line 4)

12. As per claim 3, Katsuki discloses an array-type processor according to claim 1, wherein said event distributing means is constituted by dedicated event communication buses that connect said plurality of state control units. (Col. 7 line 47 – col. 8 line 4)

13. As per claim 4, Katsuki discloses an array-type processor according to claim 1, wherein:

data buses for transmitting processing data of said plurality of processor elements are arranged in matrix form; (Fig. 2 buses 48 and 50)

a plurality of switch elements (Fig. 2 router 42), which switch-control a wiring configuration of said data buses in accordance with instruction codes that are individually set as data, (Col. 8 lines 26-28)

are arranged in matrix form together with said processor elements; *Fig. 2 discloses routers located at every bus junction, in matrix form.*

said state control units successively switch said instruction codes of said plurality of processor elements and said plurality of switch elements; *The examiner asserts that the controllers issue code to the processors and control the routers upon receiving new instructions to do so.*

and said event distributing means is constituted by said data buses that are switch-controlled by said switch elements. (Col. 7 line 47 – col. 8 line 4 and Col. 8 lines 26-28)

14. As per claim 5, Katsuki discloses an array-type processor according to claim 2, wherein all of said plurality of state control units are interconnected by said event distributing means. *The examiner asserts that Fig. 2 illustrates all controllers connected by buses 50 and 48.*

15. As per claim 6, Katsuki discloses an array-type processor according to claim 2, wherein: said plurality of state control units are arranged in rows and columns (Fig. 1); and said state control units are connected by said event distributing means to a portion of said state control units that are located in a vicinity. *The examiner asserts that Fig. 2 illustrates all controllers connected by buses 50 and 48.*

16. As per claim 7, Katsuki discloses an array-type processor according to claim 6, wherein: said plurality of state control units are arranged in rows and columns (Fig. 1), and said state control units are connected by said event distributing means to state control units that are located in eight directions in the vicinity. *The examiner asserts that Fig. 2 illustrates all controllers connected by buses 50 and 48. Further, col. 6 lines 7-9 dictate that any controller can send data to any other controller, no matter what direction the destination controller lies.*

17. As per claim 8, Katsuki discloses an array-type processor according to claim 6, wherein: said plurality of state control units are arranged in rows and columns (Fig. 1); and said state control units are connected by said event distributing means to said state control units that are adjacent in four row and column directions. *The examiner asserts that Fig. 2 illustrates all controllers connected by buses 50 and 48. Further, col. 6 lines 7-9 dictate that any controller can send data to any other controller, no matter what direction the destination controller lies.*

18. As per claims 9 and 10, Katsuki discloses an array-type processor according to claims 1 and 6, wherein: a central control unit (Fig. 2 host computer 58) is provided for distributing said event data to said plurality of state control units (Col. 6 lines 7-9); and said central control unit is connected by said event distributing means to all of said plurality of state control units. *The examiner asserts that the host is connected via buses 48, 50 and 56 according to fig. 2.*

19. As per claims 11 and 12, Katsuki discloses an array-type processor according to claims 1 and 6, wherein: an input selection means is provided for each of said state control units for selecting one from said plurality of items of event data that are simultaneously received as input by said event distributing means. *Fig. 6 illustrates a router receiving data from the buses. Col. 12 begins the description of how data is input from the control buses.*

20. As per claim 13, Katsuki discloses an array-type processor according to claim 11, wherein one item of said event data that has been selected by said input selection means is supplied as output to said event distributing means. *Data can be sent from a column to a row (or vice versa) by means of the router at the junction of the two. (Col. 12 lines 30-38)*

21. As per claim 14, Katsuki discloses an array-type processor according to claim 11, wherein output selection means is provided for each of said state control units, said output selection means selecting one from a plurality of items of said event data that are simultaneously received as input by said event distributing means and supplying these event data as output to said event distributing means. *Fig. 5 illustrates outputting data onto a row or column bus. Data can be sent from a column to a row (or vice versa) by means of the router at the junction of the two. (Col. 12 lines 30-38)*

22. As per claims 15, 16 and 17 Katsuki discloses an array-type processor according to claims 1, 6 and 11, wherein:

> said multiplicity of processor elements is divided into element areas that correspond in number to said state control units; *The examiner asserts that each processor/controller combination constitutes an element area. Col. 6 line 34 and Fig. 1 disclose processor units and controllers being in a 1:1 correspondence.*

each of said plurality of state control units is connected to said processor elements of a respective element area of said plurality of element areas; *The examiner asserts that each controller is connected to the one and only processor in its element area.*

and said event distributing means transmits said event data that are supplied as output by said processor elements of each element area to a respective state control unit of said state control units. *The examiner asserts that each controller can send data to any other controller, all of which are in other element areas. (Col. 5 lines 7-9)*

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shams et al. (U.S. Patent No. 6,145,072) disclose an interconnection matrix in an array processor allowing redirection of data from each processing element.

Pechanek et al. (U.S. Patent No. 6,606,699) disclose an array processor with processors that communicate in multiple directions.

24. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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